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Review of Study and Design of Coding and Interleaving in a MIMO-OFDM Communication System

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Abstract

This paper, presents of the review performance analysis of four different channel coding and interleaving schemes for MIMO-OFDM communications systems. A comparison is done based on the BER, hardware implementation resources requirement, and power dissipation. It also presents a memory-efficient and low-latency interleaver implementation technique for the MIMO-OFDM communication system. One aspect of the MIMO-OFDM system that has not been investigated adequately is the effect of using different combinations of the convolutional encoder and interleaver on the system performance. This works focus on a specific FEC mechanism and do not compare their schemes with other alternatives among the four possible schemes. In this paper the performance and computational complexity of the four different convolutional encoding and interleaving schemes are analyzed. The IEEE 802.16 standard is used as a reference for simulation and analysis. This is the method for interleaver design on FPGA and its memory utilization. This project work concentrate on efficient interleaver design for IEEE 802.16 system implemented on FPGA. Our goal is to achieve minimum memory usage, faster interleaving, and increased speed of the overall system. The proposed interleaver, a MIMO-OFDM based transmitter employing a double data stream 2×2 MIMO spatial multiplexing system is built.

Keywords: Channel Coding, Interleaving, MIMO-OFDM, IEEE 802.16, FEC.

Introduction

The IEEE 802.16 defines the standard for broadband wireless access covering the physical layer and medium access specifications for wireless metropolitan area networks (WMAN). The IEEE 802.16 Air Interface Standard is a technology [2] that is playing a key role in fixed broadband wireless MAN. Yu et al. [3] adopted per-antenna coding (separate encoder for each data stream) with cross-antenna interleaving (combined interleaving for all the data streams), and Haene et al. [4] used cross-antenna coding (combined encoder for all the data streams) with cross-antenna interleaving. On the other hand, Boher et al. [5] employed per-antenna coding with per-antenna interleaving (separate interleaving for each data stream), while Muller-Weinfurtner [6] used cross-antenna coding with per-antenna interleaving. However, cited works focus on a specific FEC mechanism and do not compare their schemes with other alternatives among the four possible schemes. In this paper, to the best of authors' knowledge, for the first time, the performance and computational complexity of the four different convolutional encoding and interleaving schemes are analyzed [1][7].

This paper is organized as follows. Section II presents an overview of proposed system. Section III presents the implementation details of MIMO-OFDM transmitter and Section IV concludes the paper.

System description

The basic OFDM communication system's block diagram is shown in Figure 1. The forward error correction (FEC) blocks include convolution encoding, puncturing, and interleaving. A modification of the system described in figure 1[8] is to use two separate data streams to enhance the data rate and possibly increase the number of antennas by using spatial as well as transmit diversity.

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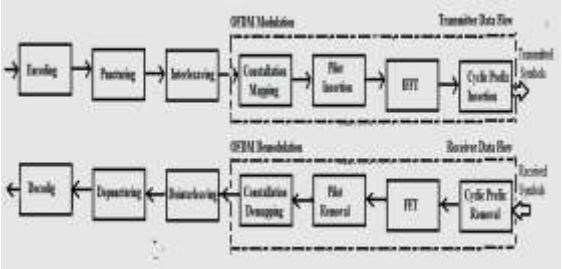

Fig. 1. OFDM communication system

The input bit stream is first encoded using punctured convolutional codes with constraint length K=7, and then interleaved to leverage frequency diversity. This is followed by constellation mapping which is BPSK, QPSK, 16-QAM, or 64-QAM depending on the signal-to- noise ratio (SNR) at the receiver. Next, the symbols are assembled, pilot symbols, and null symbols are inserted. A 256-point IFFT forms the OFDM symbol with 192 data, 8 pilots, and 56 null subcarriers forming the frequency guard bands [6]. The IFFT block computes a 256-point IFFT to form an OFDM symbol. This is the most computationally complex part of the system. A cyclic prefix (CP) is inserted at the start of every OFDM symbol to avoid inter-symbol interference in the case of any delay at the receiver. CP is the end fraction (*Tg*) of the OFDM useful symbol period (*Tb*) that is copied to its beginning and is used to collect multipath while maintaining the orthogonality of the tones. CP varies between 1/4, 1/8, 1/16, and 1/32 depending on the bandwidth used, which can vary from 1.5 to 28 MHz. The completed symbol corresponding to 320 points is then transmitted over the channel.

For the analysis and implementation in this paper, four different FEC schemes of double data stream MIMO systems are used, which are categorized as follows. Details of thes schemes have been discussed by Iqbal and Nooshabadi[8].

Case 1: Cross-antenna convolutional coding with per-antenna interleaving (CAPA), shown in Fig. 2.

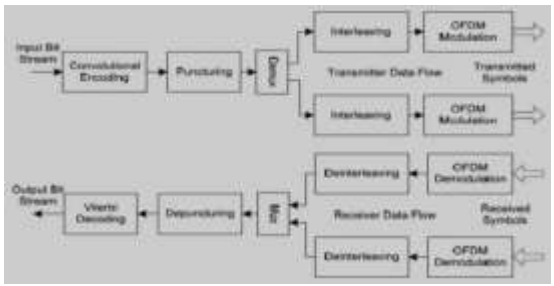

Fig. 2. Cross-antenna coding with per-antenna interleaving

Case 2: Per-antenna convolutional coding with per-antenna interleaving (PAPA), shown in Fig. 3.

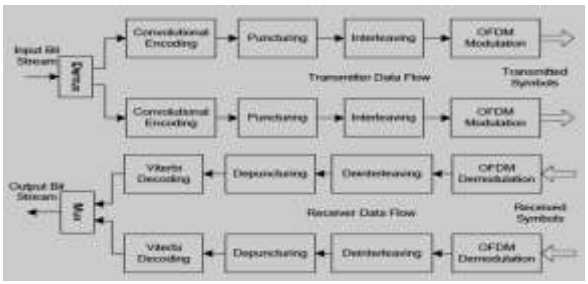

Fig. 3. Per-antenna coding with per-antenna interleaving

Case 3: Cross-antenna convolutional coding with cross-antenna interleaving (CACA),shown in Fig. 4

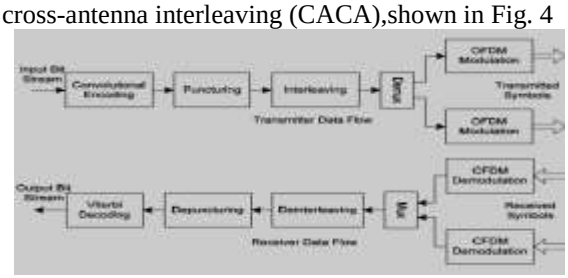

Fig. 4. Cross-antenna coding with cross-antenna interleaving

Case 4: Per-antenna convolutional coding with cross-antenna interleaving (PACA),shown in Fig. 5

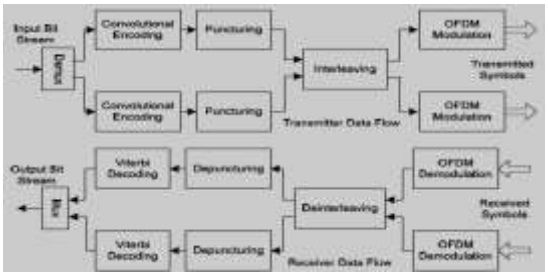

Fig. 5. Per-antenna coding with cross-antenna interleaving

In all these cases, the input data is first encoded using a convolutional encoder followed by puncturing. For this analysis, a coding rate of 1/2 is used for BPSK modulation, while coding rate of 3/4 is used for QPSK, 16-QAM, and 64- QAM. Next step is interleaving, which is implemented using a block interleaver, whose size varies according to the modulation scheme used and the system configuration [5]. The receiver performs these functions in reverse order to retrieve the data as shown in Fig. 1. A memoryless AWGN channel and an ideal channel gain of unity for each subcarrier are used, which eliminates the need for channel estimation an carrier recovery.

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System implementation

To analyze the hardware implication of various coding and interleaving schemes considered in this paper, in this section, the IEEE 802.16-2009 (WiMAX) [2] transmitter is modeled in VHDL.

A. Convolutional Encoder

As shown in Fig. 6, convolutional encoder is implemented using a 6-bit long shift register and *XOR* gates. Two outputs, *X* and *Y* are formed as *modulo2* sums and generated using *XOR* operations as described in IEEE Std. 802.16-2009 [2].

B. Puncturing

Puncturing is implemented using shift registers. For QPSK, *X* and *Y* outputs of the encoders feed two 3-bit shift registers. From each shift register one bit is punctured every 3 clock cycles to create two 2-bit symbols. Each symbol is sent on each data stream for QPSK mapping. For 16-QAM, the same procedure is employed using 6-bit shift registers to *X* and *Y* outputs of the encoders. The puncturing drops two bits from each shift register every 6 clock cycles. Two 4-bit symbols are sent to two data streams for 16-QAM mapping. For 64-QAM, the same procedure is used with 9-bit shift registers as we need 12 bits at the output to generate two 6-bit symbols to send on each data stream.

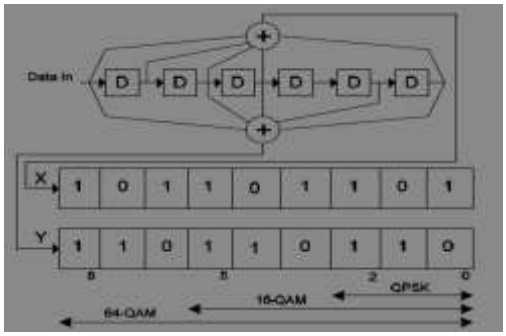

Fig. 6. Convolutional encoding and puncturing block

C. Interleaver

The interleaver is implemented using the dedicated RAM blocks (BRAM) or distributed RAM (DisRAM) on the FPGA fabric plus a state machine for the address generator for read/write operations. Double buffering technique is used to implement the interleaver to eliminate the delay in the interleaving process. After the first block of symbols is stored in the buffer, the address generator [6] starts generating read addresses and starts reading data from the buffer. In the mean -time, the second buffer is filled with incoming data and the interleaver will start reading from the second buffer after the first one is read out completely. Table I shows the buffer sizes for different interleaving schemes used in our system. The numbers of buffers increase with the increase in modulation symbol size, so that we can write/read data from them at the same time.

TABLE I: Buffer Sizes For Different Modulation Schemes:

Modulation Schemes	BPSK	QPSK	16-QAM	64-QAM
Buffer size	384	384	384	384
No of buffers	2	4	5	6

1) Interleaver for BPSK Mapping

For BPSK mapping, the interleaver is implemented using a single memory block of double the required size. For example, an interleaver of size 192 is implemented using a buffer of 384 bits as shown in table I. Incoming bits are first stored in the RAM until 192 bits are filled and then the readout is enabled. A state machine generates write addresses for the RAM to write data to it. After 192 writes to the RAM, it asserts the read enable signal and starts generating read addresses for the RAM while continuing with the write process. This way the next part of the buffer is filled when the interleaver finishes reading the first 192 bits and then it starts reading the next 192 bits.

2) Interleaver for QPSK Mapping

For QPSK mapping, the interleaver is implemented using two memory blocks of double the required size. A state machine generates a single address for the two RAMs to write data to them simultaneously. The pattern thus formed can be read out column-wise from RAM1 and RAM2 alternatively to implement the interleaver function. After 192 writes to each RAM, it asserts the read enable signals and starts generating read addresses for each RAM while continuing with the write process. The address generator generates two read addresses successively with an increment of 6, in order to read 2 locations from one RAM during one read operation. The first column of RAM1 is read first, followed by the first column of RAM2 and this process continues until the last location is read.[5] This technique enables us to write 3 bits to the buffer at the same time and read 3 bits successively to generate a 3-bit symbol for QPSK mapping.

3) Interleaver for 16-QAM Mapping

For 16-QAM mapping the interleaver is implemented using four memory blocks of double the required size. The method of read and write address generation is the

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same as explained before except the fact that now we have four separate RAMs that are first filled simultaneously and then the data is read out column-wise from RAM1, RAM2, RAM3, and RAM4 alternatively to implement the interleaver function. The address generator generates four read addresses successively with an increment of 3, in order to read 4 locations from one RAM during one read operation. This technique enables us to write 5 bits to the buffer at the same time[8] and read 5 bits successively to generate a 5-bit symbol for 16-QAM mapping.

4) Interleaver for 64-QAM Mapping

For 64-QAM mapping, the interleaver is implemented using six memory blocks (RAM1 to RAM6), which are logically partitioned into two partitions. Partition $0 \leq k < 2$ corresponds to addresses of address%2 = k. The group of six successive reads is used to generate a 6-bit symbol for 64-QAM mapping. The structures for the other modulation schemes are similar. As explained above, six memory blocks partitioned into two logical partitions are used.

D. Constellation Mapper

Constellation mapping for each scheme is implemented using a ROM which stores the pre-calculated I (real) and Q (imaginary) output values for each input symbol. Two ROMs, one for each I and Q values are used, having a 16-bit output with 14 fractional bits, 1 bit for magnitude, and 1 sign bit. The constellation mapping block for each scheme, implements the mapping technique as explained in the IEEE Std. 802.16-2009 [2].

E. OFDM Modulator

The OFDM modulator needs to produce 320 (IFFT + CP) symbols. The incoming data from the interleaver should be buffered before it is consumed by the IFFT module, as 320 output symbols per every 192 input symbols should be produced. The OFDM modulator block inserts 8 pilot, 1 DC, and 55 null subcarriers, and produces a cyclic prefix of 64 symbols during the input time of 192 input symbols to this block.

Conclusion

In this paper, an efficient way to design the OFDM transmitter on FPGA is presented. A special design method is used to implement the interleaver with minimum memory requirement and initial latency. This approach can also be used to design other high-speed communication systems or to improve their speed. The proposed optimizations can be utilized in real time applications since they only require to replace the current interleaving parameters and do not involve any hardware alteration. The transmitter using different modulation schemes will have been coded and stimulated and compares with respect to area, frequency and power utilizations.

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